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APPLICANTS Hisashi Ohtani, Kanagawa, JAPAN;				
** CONTINUING DATA ***** This application is a DIV. of 09/967,697 09/28/2001 PAT 6,657,228 which is a CON of 08/862,895 05/23/1997 PAT 6,316,787				
** FOREIGN APPLICATIONS ***** <i>Yoshiyuki</i> JAPAN 8-165272 06/04/1996				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 12/01/2003				
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Verified and Acknowledged <i>M. Sato</i> <i>Initials</i> Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 11	TOTAL CLAIMS 24
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TITLE Semiconductor integrated circuit and fabrication method thereof				
FILING FEE	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time)	